

CLAIMS

What is claimed is:

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A digital cross connect comprising:
plurals switching stages, each stage having plural switches receiving
5 plurals frames of time multiplexed input data and switching the data in time and
space;
a frame counter at each switch synchronized to a frame clock; and
a master switch within the plural switching stages from which the frame
clock is propagated to downstream switches and from output stages to input
10 stages.

2. A digital cross connect as claimed in claim 1 wherein propagation of the frame
clock is matched to data distribution between the switches.

3. A digital cross connect as claimed in claim 2 wherein the frame clock is derived
from a frame of data.

15 4. A cross connect as claimed in claim 3 wherein the frame clock is derived from
an A1 byte of a SONET frame.

5. A cross connect as claimed in claim 3 wherein each switch selects between an
external frame clock input and a frame clock derived from one of plural frames
of data.

20 6. A cross connect as claimed in claim 5 wherein the frame counter of each switch
is aligned to a defined offset from the selected frame clock.

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7. A cross connect as claimed in claim 6 wherein a switch selects between one of plural redundant frame clock inputs propagated from the master switch, each with a respective defined offset.

8. A cross connect as claimed in claim 1 wherein a switch frame counter is aligned to a defined offset from the frame clock.

9. A cross connect as claimed in claim 8 wherein a switch comprises multiple frame counters having different alignments.

10. A cross connect as claimed in claim 9 wherein each switch includes two frame counters.

11. A cross connect as claimed in claim 9 wherein a single switch module implements portions of two stages of the cross connect using respective frame counters.

12. A cross connect as claimed in claim 1 wherein the master switch is in a middle stage.

13. A method of providing a digital cross connect comprising:
providing plural switching stages, each stage having plural switches which receive plural frames of time multiplexed input data and which switch the data in time and space;
propagating a frame clock from a master switch within the plural switching stages to downstream switches and from output stages to input stages; and
synchronizing a frame counter at each switch to the propagated frame clock.

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14. A method as claimed in claim 13 wherein propagation of the frame clock is matched to data distribution between the switches.
15. A method as claimed in claim 14 wherein the frame clock is derived from a frame of data.
- 5 16. A method as claimed in claim 15 wherein the frame clock is derived from an A1 byte of a SONET frame.
17. A method as claimed in claim 15 wherein each switch selects between an external frame clock input and a frame clock derived from one of plural frames of data.
- 10 18. A method as claimed in claim 17 wherein the frame counter of each switch is aligned to a defined offset from the selected frame clock.
19. A method as claimed in claim 17 wherein a switch selects between one of plural redundant frame clock inputs propagated from the master switch, each with a respective defined offset.
- 15 20. A method as claimed in claim 13 wherein a switch frame counter is aligned to a defined offset from the frame clock.
21. A method as claimed in claim 20 further comprising generating plural frame counters at a switch, each frame counter aligned to a different offset from the frame clock.
- 20 22. A method as claimed in claim 21 wherein each switch includes two frame counters.

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23. A method as claimed in claim 21 wherein a single switch module implements portions of two stages of the cross connect using respective frame counters.

24. A method as claimed in claim 13 wherein the master switch is in a middle stage.

25. A digital cross connect comprising:

5 plural switching stages, each stage having plural switching means for receiving plural frames of the time multiplexed data and switching the data in time and space;

 frame counter means at each switch for providing a frame count synchronized to a frame clock; and

10 master switch means within the plural switching stages for propagating the frame clock to downstream switches and from output stages to input stages.